EPSON

E0C6S32

4-bit Single Chip Microcomputer

Low Voltage Operation Products

- Core CPU Architecture
- SVD Circuit/Comparator
- Event Counter

■ DESCRIPTION

The E0C6S32 is an advanced single-chip CMOS 4-bit microcomputer consisting of the E0C6200A 4-bit core CPU. It also contains the ROM, RAM, LCD driver, event counter, SVD circuit, stopwatch counter, and time base counter. With wide voltage range and low power consumption, the E0C6S32 provides an excellent solution for the low-power consumption systems with manganese dry cell.

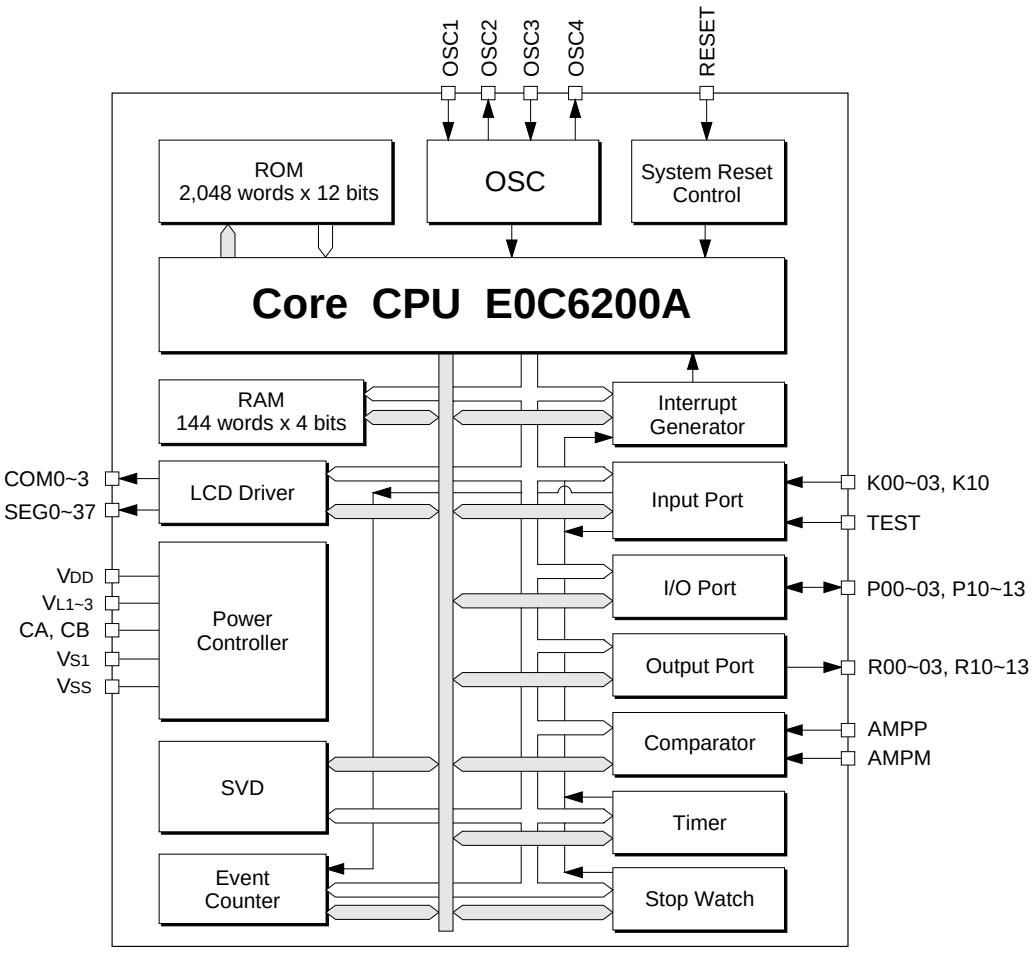
■ FEATURES

- CMOS LSI 4-bit parallel processing
- Clock ..... 32.768kHz (Typ.)/1MHz (Typ.) (selectable by software)
- Instruction set ..... 100 instructions
- Instruction cycle time ..... 153µsec, 214µsec or 366µsec at 32kHz (depending on instruction)
  5µsec, 7µsec or 12µsec at 1MHz (depending on instruction)
- ROM capacity ..... 2,048 × 12 bits
- RAM capacity ..... 144 × 4 bits
- Input port ..... 5 bits (pull-down resistors are available by mask option)
- Output port ..... 4 bits (general purpose)
  2 bits (buzzer output): BZ, $\overline{BZ}$
  1 bit (lamp output)
  1 bit (clock output)
- I/O port ..... 8 bits
- LCD driver ..... 38 segments × 2, 3 or 4 commons
  (1/2, 1/3 or 1/4 duty is selectable by mask option)
- Built-in time base counter
- Built-in stopwatch counter
- Built-in watchdog timer
- Event counter ..... 8 lines
- Built-in AMP ..... Operational AMP for MOS input analog comparator
- Built-in SVD ..... 1.2 ± 0.1V/2.4 ± 0.1V (supply voltage detector)
- Interrupts ..... External : Input interrupt 2 lines
  Internal : Timer interrupt 1 line
  Stopwatch interrupt 1 line
- Current consumption ..... E0C6SL32/6SB32 HALT mode (32kHz) : 1.0µA (Typ.)
  E0C6S32 HALT mode (32kHz) : 1.2µA (Typ.)
  E0C6SA32 HALT mode (32kHz) : 1.5µA (Typ.)
  OPERATING mode (1MHz) : 300µA (Typ.)
- Package ..... QFP5-80pin (plastic), QFP14-80pin (plastic)
  Die form

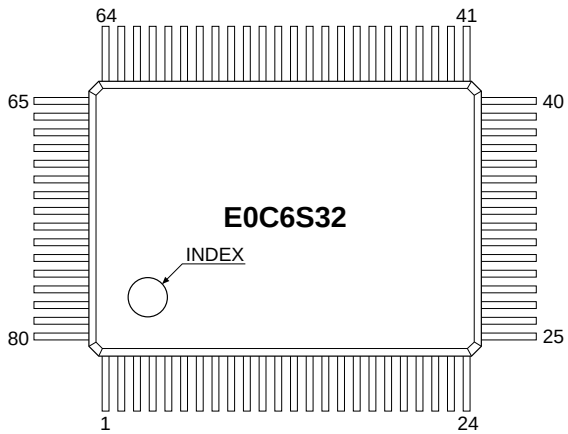
■ LINE UP

Model	Supply voltage	Clock
E0C6SL32	1.5V (0.9V to 1.8V)	32kHz (Crystal oscillation)
E0C6S32	3.0V (1.8V to 3.6V)	32kHz (Crystal oscillation)
E0C6SA32	3.0V (2.2V to 3.6V)	32kHz (Crystal oscillation) & 1MHz (Ceramic or CR oscillation)
E0C6SB32	Wide voltage (0.9V to 3.6V)	32kHz (Crystal oscillation)

■ BLOCK DIAGRAM



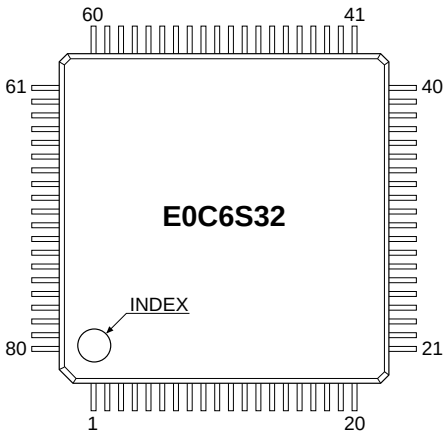
■ PIN CONFIGURATION



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	SEG17	21	SEG36	41	R00	61	COM2
2	TEST	22	SEG37	42	R12	62	COM1
3	SEG18	23	AMPP	43	R11	63	COM0
4	SEG19	24	AMPM	44	R10	64	SEG0
5	SEG20	25	K10	45	R13	65	SEG1
6	SEG21	26	K03	46	V_{SS}	66	SEG2
7	SEG22	27	K02	47	RESET	67	SEG3
8	SEG23	28	K01	48	OSC4	68	SEG4
9	SEG24	29	K00	49	OSC3	69	SEG5
10	SEG25	30	P03	50	V_{S1}	70	SEG6
11	SEG26	31	P02	51	OSC2	71	SEG7
12	SEG27	32	P01	52	OSC1	72	SEG8
13	SEG28	33	P00	53	V_{DD}	73	SEG9
14	SEG29	34	P13	54	V_{L3}	74	SEG10
15	SEG30	35	P12	55	V_{L2}	75	SEG11
16	SEG31	36	P11	56	V_{L1}	76	SEG12
17	SEG32	37	P10	57	N.C.	77	SEG13
18	SEG33	38	R03	58	CB	78	SEG14
19	SEG34	39	R02	59	CA	79	SEG15
20	SEG35	40	R01	60	COM3	80	SEG16

N.C. = No Connection

QFP14-80pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	AMPP	21	R11	41	COM0	61	SEG18
2	AMPM	22	R10	42	SEG0	62	SEG19
3	K10	23	R13	43	SEG1	63	SEG20
4	K03	24	V_{SS}	44	SEG2	64	SEG21
5	K02	25	RESET	45	SEG3	65	SEG22
6	K01	26	OSC4	46	SEG4	66	SEG23
7	K00	27	OSC3	47	SEG5	67	SEG24
8	P03	28	V_{S1}	48	SEG6	68	SEG25
9	P02	29	OSC2	49	SEG7	69	SEG26
10	P01	30	OSC1	50	SEG8	70	SEG27
11	P00	31	V_{DD}	51	SEG9	71	SEG28
12	P13	32	V_{L3}	52	SEG10	72	SEG29
13	P12	33	V_{L2}	53	SEG11	73	SEG30
14	P11	34	V_{L1}	54	SEG12	74	SEG31
15	P10	35	N.C.	55	SEG13	75	SEG32
16	R03	36	CB	56	SEG14	76	SEG33
17	R02	37	CA	57	SEG15	77	SEG34
18	R01	38	COM3	58	SEG16	78	SEG35
19	R00	39	COM2	59	SEG17	79	SEG36
20	R12	40	COM1	60	TEST	80	SEG37

N.C. = No Connection

■ PIN DESCRIPTION

Pin name	Pin No.		In/Out	Function
	QFP5-80pin	QFP14-80pin		
V_{DD}	53	31	I	Power source (+) terminal
V_{SS}	46	24	I	Power source (-) terminal
V_{S1}	50	28	O	Oscillation and internal logic system regulated voltage output terminal
V_{L1}	56	34	O	LCD system regulated voltage output terminal (approx. -1.05 V)
V_{L2}	55	33	O	LCD system booster output terminal (V_{L1} x 2)
V_{L3}	54	32	O	LCD system booster output terminal (V_{L1} x 3)
CA, CB	57, 58	35, 36	–	Booster capacitor connecting terminal
OSC1	52	30	I	Crystal oscillation input terminal
OSC2	51	29	O	Crystal oscillation output terminal
OSC3	49	27	I	Ceramic or CR oscillation input terminal (Switchable by mask option, 6SA32 only)
OSC4	48	26	O	Ceramic or CR oscillation output terminal (Switchable by mask option, 6SA32 only)
K00–K03, K10	25–29	3–7	I	Input terminal
P00–P03, P10–P13	30–37	8–15	I/O	I/O terminal
R00–R03	38–41	16–19	O	Output terminal
R10	44	22	O	Output terminal (DC or $\overline{BZ}$ output may be selected by mask option)
R13	45	23	O	Output terminal (DC or $\overline{BZ}$ output may be selected by mask option)
R11	43	21	O	Output terminal
R12	42	20	O	Output terminal (DC or FOUT output may be selected by mask option)
AMPP	23	1	I	Analog comparator non-inverted input terminal
AMPM	24	2	I	Analog comparator inverted input terminal
SEG0–37	1, 3–22, 64–80	42–59, 61–80	O	LCD segment output terminal (Convertible to DC output by mask option)
COM0–3	60–63	38–41	O	LCD common output terminal
RESET	47	25	I	Initial reset input terminal
TEST	2	60	I	Test input terminal

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

E0C6S32/6SA32/6SB32

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-5.5 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.5	V
Permissible total output current *1	ΣI_{VSS}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

∗1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
∗2: In case of plastic package (QFP5-80pin, QFP14-80pin).

E0C6SL32

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-2.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.5	V
Permissible total output current *1	ΣI_{VSS}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / Time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW

∗1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
∗2: In case of plastic package (QFP5-80pin, QFP14-80pin).

● Recommended Operating Conditions

E0C6S32

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-3.6	-3.0	-1.8	V
Oscillation frequency	f_{OSC1}		–	32.768	–	kHz

E0C6SL32

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-1.8	-1.5	-1.1	V
		V_{DD}=0V, With software control *1	-1.8	-1.5	-0.9 *2	V
		V_{DD}=0V, When the analog comparator is used	-1.8	-1.5	-1.2	V
Oscillation frequency	f_{OSC1}		–	32.768	–	kHz

∗1: When switching to heavy load protection mode. Note, however, that the ON time for BLS in the heavy load protection must be limited to 10 msec per second of operation time.
∗2: The possibility of LCD panel display differs depending on the characteristics of the LCD panel.

E0C6SB32

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-3.6	-1.5	-1.1	V
		V_{DD}=0V, With software control *1	-3.6	-1.5	-0.9 *2	V
		V_{DD}=0V, When the analog comparator is used	-3.6	-1.5	-1.2	V
Oscillation frequency	f_{OSC1}		–	32.768	–	kHz

∗1: When switching to heavy load protection mode. Note, however, that the ON time for BLS in the heavy load protection must be limited to 10 msec per second of operation time.
∗2: The possibility of LCD panel display differs depending on the characteristics of the LCD panel.

E0C6SA32

(Ta=-20 to 70°C)

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	-3.6	-3.0	-1.8	V
Oscillation frequency (1)	f_{OSC1}		–	32.768	–	kHz
Oscillation frequency (2)	f_{OSC3}	duty 50±5%	300	1000	1300	kHz

● DC Characteristics

E0C6S32/6SA32

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–K03, K10 P00–P03, P10–P13	0.2•V_{SS}		0	V
High level input voltage (2)	V_{IH2}		RESET, TEST	0.1•V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–K03, K10 P00–P03, P10–P13	V_{SS}		0.8•V_{SS}	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	V_{SS}		0.9•V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V, No pull down resistor	K00–K03, K10 P00–P03, P10–P13 AMPP, AMPM	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V, With pull down resistor	K00–K03, K10	4		40	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V, With pull down resistor	P00–P03, P10–P13 RESET, TEST	25		150	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–K03, K10 P00–P03, P10–P13 AMPP, AMPM RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1•V_{SS}	R10, R11, R13			-1.8	mA
High level output current (2)	I_{OH2}	V_{OH2}=0.1•V_{SS}	R00–R03, R12 P00–P03, P10–P13			-0.9	mA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9•V_{SS}	R10, R11, R13	4.0			mA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9•V_{SS}	R00–R03, R12 P00–P03, P10–P13	3.0			mA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–COM3			-3	µA
	I_{OL3}	V_{OL3}=V_{L3}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=-0.05V	SEG0–SEG37			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.1•V_{SS}	SEG0–SEG37			-200	µA
	I_{OL5}	V_{OL5}=0.9•V_{SS}		200			µA

E0C6SL32/6SB32

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}		K00–K03, K10 P00–P03, P10–P13	0.2•V_{SS}		0	V
High level input voltage (2)	V_{IH2}		RESET, TEST	0.1•V_{SS}		0	V
Low level input voltage (1)	V_{IL1}		K00–K03, K10 P00–P03, P10–P13	V_{SS}		0.8•V_{SS}	V
Low level input voltage (2)	V_{IL2}		RESET, TEST	V_{SS}		0.9•V_{SS}	V
High level input current (1)	I_{IH1}	V_{IH1}=0V, No pull down resistor	K00–K03, K10 P00–P03, P10–P13 AMPP, AMPM	0		0.5	µA
High level input current (2)	I_{IH2}	V_{IH2}=0V, With pull down resistor	K00–K03, K10	2		16	µA
High level input current (3)	I_{IH3}	V_{IH3}=0V, With pull down resistor	P00–P03, P10–P13 RESET, TEST	9		60	µA
Low level input current	I_{IL}	V_{IL}=V_{SS}	K00–K03, K10 P00–P03, P10–P13 AMPP, AMPM RESET, TEST	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{OH1}=0.1•V_{SS}	R10, R11, R13			-300	µA
High level output current (2)	I_{OH2}	V_{OH2}=0.1•V_{SS}	R00–R03, R12 P00–P03, P10–P13			-150	µA
Low level output current (1)	I_{OL1}	V_{OL1}=0.9•V_{SS}	R10, R11, R13	1,400			µA
Low level output current (2)	I_{OL2}	V_{OL2}=0.9•V_{SS}	R00–R03, R12 P00–P03, P10–P13	700			µA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–COM3			-3	µA
	I_{OL3}	V_{OL3}=V_{L3}+0.05V		3			µA
Segment output current (during LCD output)	I_{OH4}	V_{OH4}=-0.05V	SEG0–SEG37			-3	µA
	I_{OL4}	V_{OL4}=V_{L3}+0.05V		3			µA
Segment output current (during DC output)	I_{OH5}	V_{OH5}=0.1•V_{SS}	SEG0–SEG37			-100	µA
	I_{OL5}	V_{OL5}=0.9•V_{SS}		100			µA

● Analog Circuit Characteristics and Current Consumption

E0C6S32 (Normal Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		0.65	2.0	µA
		During operation *1			2.0	4.0	µA

*1: The SVD circuit and analog comparator are in the OFF status.

E0C6S32 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		11.2	34.0	µA
		During operation *1			14.5	40.0	µA

*1: The SVD circuit is in the ON status (HLMOD="1", BLS="0"). The analog comparator is in the OFF status.

E0C6SL32 (Normal Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.1V, V_{IM}=V_{IP}±30mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		0.65	1.5	µA
		During operation *1			2.0	4.0	µA

*1: The SVD circuit and analog comparator are in the OFF status.

E0C6SL32 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.85	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.85	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.1V, V_{IM}=V_{IP}±30mV				3	mS
Current consumption	I_{OP}	During HALT *1	Without panel load		11.2	34.0	µA
		During operation *1			14.5	40.0	µA

*1: The SVD circuit is in the ON status (HLMOD="1", BLS="0"). The analog comparator is in the OFF status.

E0C6SB32 (Normal Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.1V, V_{IM}=V_{IP}±30mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		0.65	1.5	µA
		During operation *1			2.0	4.0	µA

*1: The SVD circuit and analog comparator are in the OFF status.

E0C6SB32 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.85	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.85	V
SVD voltage	V_{SVD}			-1.30	-1.20	-1.10	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					20	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.1V, V_{IM}=V_{IP}±30mV				3	mS
Current consumption	I_{OP}	During HALT *1	Without panel load		11.2	34.0	µA
		During operation *1			14.5	40.0	µA

*1: The SVD circuit is in the ON status (HLMOD="1", BLS="0"). The analog comparator is in the OFF status.

E0C6SA32 (Normal Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		1.5	3.0	µA
		During operation *1	OSCC="0"		4.0	8.0	µA
		During operation at 1MHz *1	Without panel load		150	300	µA

*1: The SVD circuit and analog comparator are in the OFF status.

E0C6SA32 (Heavy Load Protection Mode)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, C_G=25pF, V_{S1}/V_{L1}–V_{L3} are internal voltage, C1–C5=0.1µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Internal voltage	V_{L1}	Connect 1MΩ load resistor between V_{DD} and V_{L1} (without panel load)		-1.15	-1.05	-0.95	V
	V_{L2}	Connect 1MΩ load resistor between V_{DD} and V_{L2} (without panel load)		2•V_{L1} -0.1		2•V_{L1} ×0.9	V
	V_{L3}	Connect 1MΩ load resistor between V_{DD} and V_{L3} (without panel load)		3•V_{L1} -0.1		3•V_{L1} ×0.9	V
SVD voltage	V_{SVD}			-2.55	-2.40	-2.25	V
SVD circuit response time	t_{SVD}					100	µS
Analog comparator input voltage	V_{IP}	Noninverted input (AMPP)		V_{SS}+0.3		V_{DD}-0.9	V
	V_{IM}	Inverted input (AMPM)					
Analog comparator offset voltage	V_{OF}					10	mV
Analog comparator response time	t_{AMP}	V_{IP}=-1.5V, V_{IM}=V_{IP}±15mV				3	mS
Current consumption	I_{OP}	During HALT	Without panel load		60	110	µA
		During operation *1	OSCC="0"		65	120	µA
		During operation at 1MHz *1	Without panel load		200	330	µA

*1: The SVD circuit is in the ON status (HLMOD="1", BLS="0"). The analog comparator is in the OFF status.

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

E0C6S32 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	t_{sta}≤5sec (V_{SS})	-1.8			V
Oscillation stop voltage	Vstp	t_{stp}≤10sec (V_{SS})	-1.8			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-1.8 to -3.6V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(V_{SS})			-3.6	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

E0C6SL32 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (Vss)	-1.1			V
Oscillation stop voltage	Vstp	tstp≤10sec (Vss)	-1.1(-0.9)*1			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-1.1 to -1.8V (-0.9) *1			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(Vss)			-1.8	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

*1: Items enclosed in parentheses ( ) are those used when operating at heavy load protection mode.
Note, however, that the ON time for BLS must be limited to 10 msec per second of operation time.

E0C6SB32 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-1.5V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (Vss)	-1.1			V
Oscillation stop voltage	Vstp	tstp≤10sec (Vss)	-1.1(-0.9)*1			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-1.1 to -3.6V (-0.9) *1			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(Vss)			-3.6	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

*1: Items enclosed in parentheses ( ) are those used when operating at heavy load protection mode.
Note, however, that the ON time for BLS must be limited to 10 msec per second of operation time.

E0C6SA32 (Crystal oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R (C_I=35kΩ), C_G=25pF, C_D=built-in, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	tsta≤5sec (Vss)	-1.8			V
Oscillation stop voltage	Vstp	tstp≤10sec (Vss)	-1.8			V
Built-in capacitance (drain)	C_D	Including the parasitic capacity inside the IC		20		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -3.6V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustment range	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	(Vss)			-3.6	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{SS}	200			MΩ

E0C6SA32 (CR oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, R_{CR}=33kΩ, Ta=25°C)

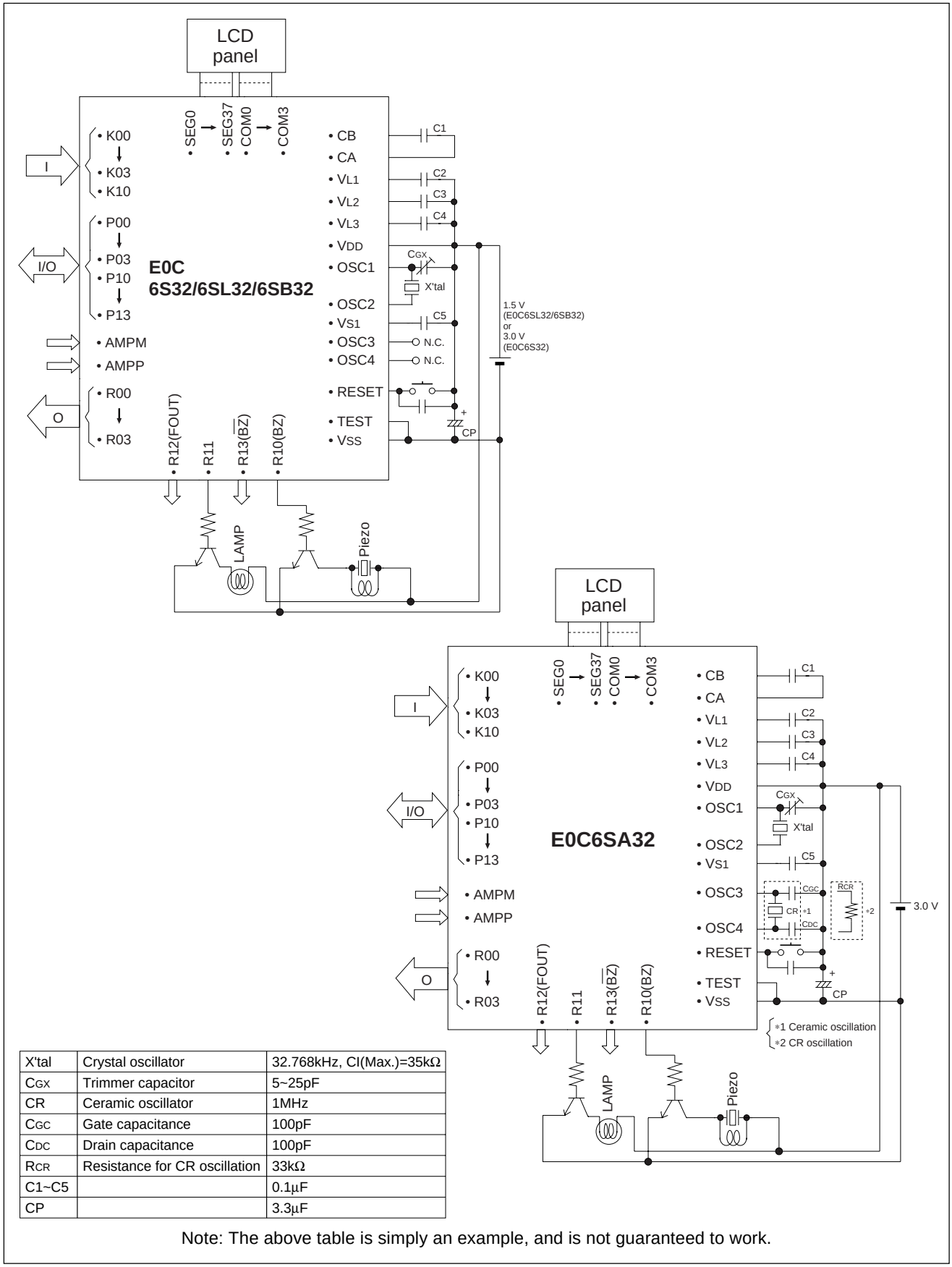
Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency dispersion	f_{OSC3}		-30	1MHz	30	%
Oscillation start voltage	Vsta	(Vss)	-1.8			V
Oscillation start time	tsta	V_{SS}=-2.2 to -3.6V			3	mS
Oscillation stop voltage	Vstp	(Vss)	-1.8			V

E0C6SA32 (Ceramic oscillation circuit)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, ceramic oscillation: 1MHz, C_{GC}=C_{DC}=100pF, Ta=25°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start voltage	Vsta	(Vss)	-1.8			V
Oscillation start time	tsta	V_{SS}=-2.2 to -3.6V			5	mS
Oscillation stop voltage	Vstp	(Vss)	-1.8			V

■ BASIC EXTERNAL CONNECTION DIAGRAM

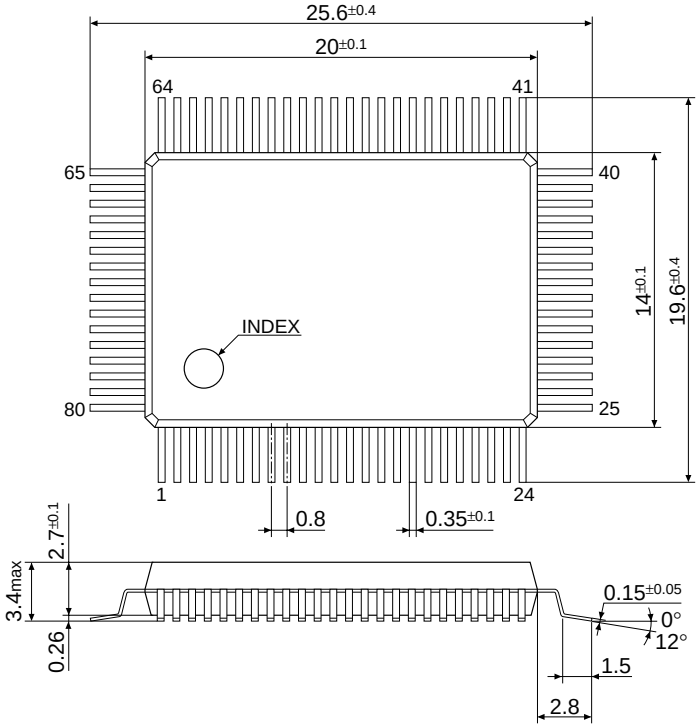


X'tal	Crystal oscillator	32.768kHz, CI(Max.)=35kΩ
CGX	Trimmer capacitor	5~25pF
CR	Ceramic oscillator	1MHz
CGC	Gate capacitance	100pF
CDC	Drain capacitance	100pF
RCR	Resistance for CR oscillation	33kΩ
C1~C5		0.1µF
CP		3.3µF

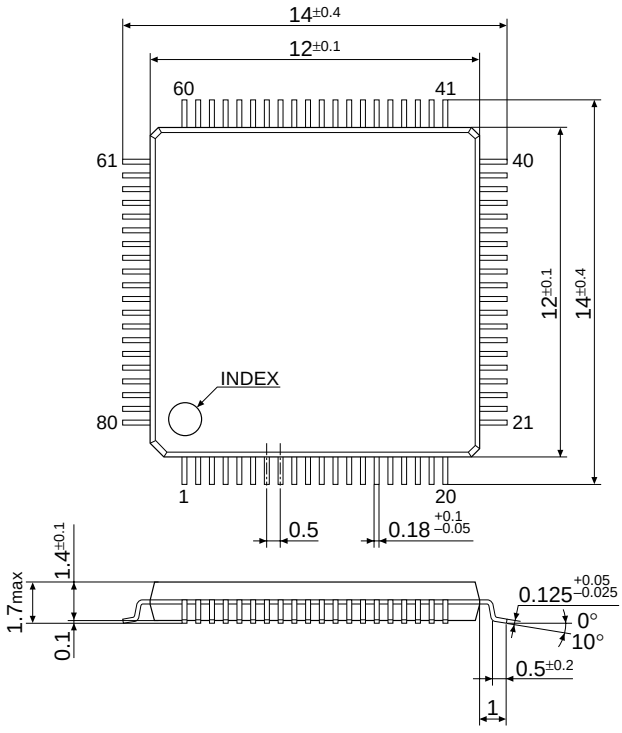
Note: The above table is simply an example, and is not guaranteed to work.

■ PACKAGE DIMENSIONS

Plastic QFP5-80pin



Plastic QFP14-80pin



Unit: mm

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